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EEC 180B

Lab 4 Report

1. Record the delay from the rising edge of the clock to the “Done” signal and include it

in your report.

3027.137 ns (posedge Done) - 3020 ns (posedge Clock) = 7.137 ns

2. Give one example of the difference between what you see in the waveforms produced

during timing simulation and functional simulation.

Functional simulation does not include the delays present in the timing simulation.

1. What are tsu, tpd, tco and th?

tsu = 5.856 ns

tpd = 15.137 ns

tco = 11.596 ns

th = -0.064 ns

2. What is the critical path of your circuit and the maximum frequency of operation?

KEY[0] to HEX3[0] or Resetn to MSB of Product, max frequency is 233.43 MHz.

3. Is the critical path consistent with your design?

Yes? It’s plausible that percolating the reset signal would take longer than the effects of the clock changing.

4. Change the maximum clock frequency constrain to 80 MHz.

Okay.

5. Recompile your design.

Did it.

6. What is the critical path of your circuit? Explain if there is any difference.

Critical path is now KEY[0] to HEX1[1]. Now there is a Clock hold time that affects the critical path.

1. Compare the power consumption of 8-bit and 16-bit Booth multiplier designs. This

involves changing the parameter “n” in your design from 8 to 16 and repeating the steps.

16-bit: 141.92 mW

8-bit: 136.7 mW

16-bit multiplier has more going on, so the power consumption has increased by 3.82%.